

# AMD BRAZOS Muxless Discrete/UMA Schematics Document

## AMD Ontario CPU FT1

## AMD GPU Seymour XT S3

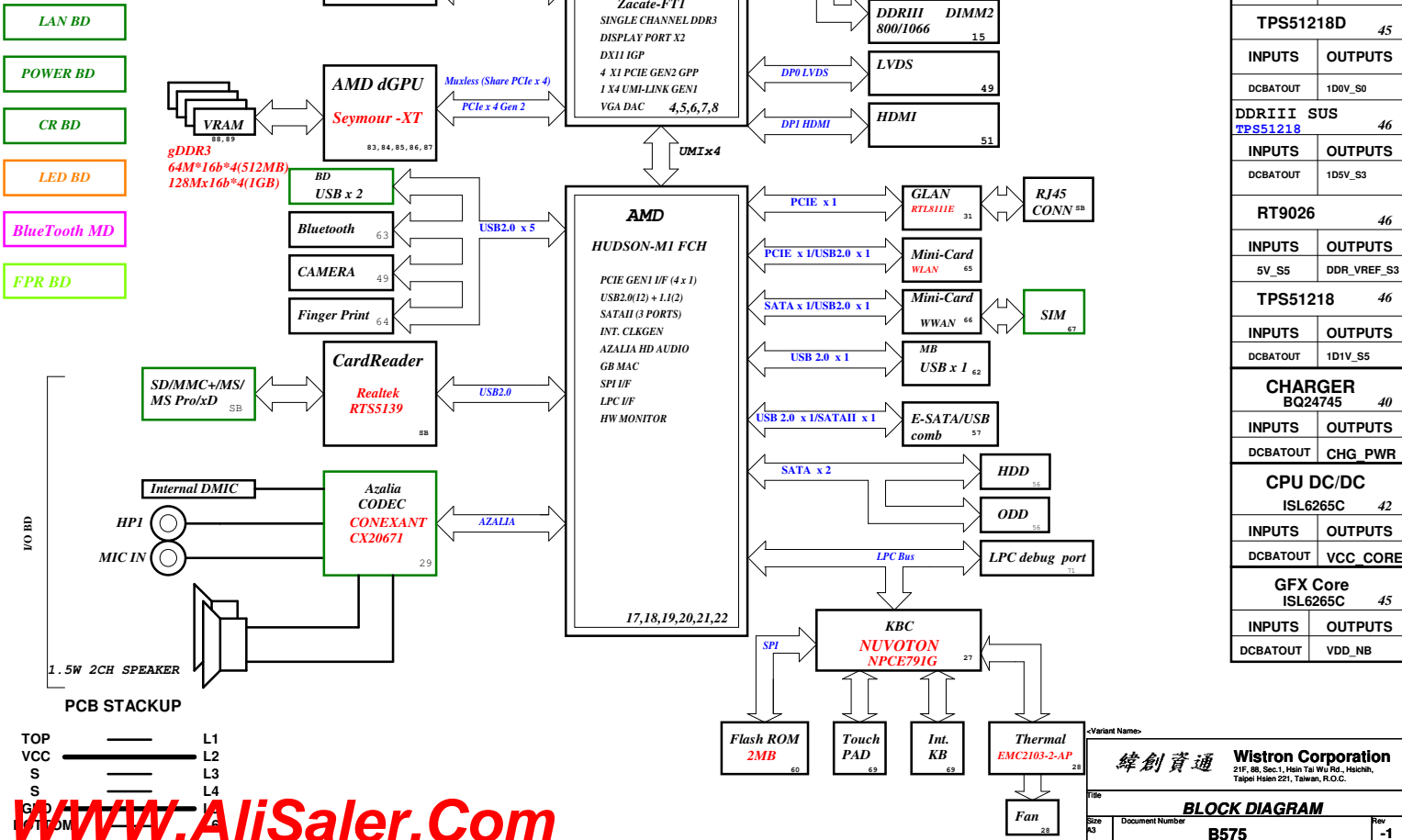
### 2010-12-01

### REV : SA

*DY :None Installed*  
*UMA:UMA platform installed*  
*PARK:DIS PARK platform installed*  
*MADISON:DIS MADISON platform installed*  
*Colay :Manual modify BOM*  
*MUX : PX*  
*ROB:ROBSON*

PROJECT CODE : 91.4PN01.001  
PCB P/N : 10332  
REVISION : SA

# Block Diagram



VGA

RT8208B

92

INPUTS

OUTPUTS

DCBATOUT

VGA\_CORE\_FWR

AMD GPU CORE

TPS51218D

47

INPUTS

OUTPUTS

DCBATOUT

1D8V\_S0

SYSTEM DC/DC

TPS51123

41

INPUTS

OUTPUTS

DCBATOUT

5V\_S5  
3D3V\_S5  
5V\_AUX\_S5  
3D3V\_AUX\_S5

TPS51218D

45

INPUTS

OUTPUTS

DCBATOUT

1D0V\_S0

DDR III SUS

TPS51218

46

INPUTS

OUTPUTS

DCBATOUT

1D5V\_S3

RT9026

46

INPUTS

OUTPUTS

5V\_S5

DDR\_VREF\_S3

TPS51218

46

INPUTS

OUTPUTS

DCBATOUT

1D1V\_S5

CHARGER

BQ24745

40

INPUTS

OUTPUTS

DCBATOUT

CHG\_PWR

CPU DC/DC

ISL6265C

42

INPUTS

OUTPUTS

DCBATOUT

VCC\_CORE

GFX Core

ISL6265C

45

INPUTS

OUTPUTS

DCBATOUT

VDD\_NB

J45

ONN

5B

SIM

67

ug port

71

PCB STACKUP

TOP	---	L1
VCC	---	L2
S	---	L3
S	---	L4
GND	---	L5
INT. DOM	---	L6

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REQUIRED SYSTEM STRAPS ?

	AZ_SDOUT	PCI_CLK1	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1	LPC_CLK2
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT	Enable boot timer function
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)	Disable boot fail timer function DEFAULT

USB Table

Pair	Device
0	Internal #3 (MB)
1	WLAN/WIMAX
2	WWAN
3	E-SATS/LUSB
4	BLUETOOTH
5	External #1 (IO BD)
6	External #2 (IO BD)
7	CAMERA (HS)
8	Finger Print
9	CardReader
10	NC
11	NC
12	NC
13	NC

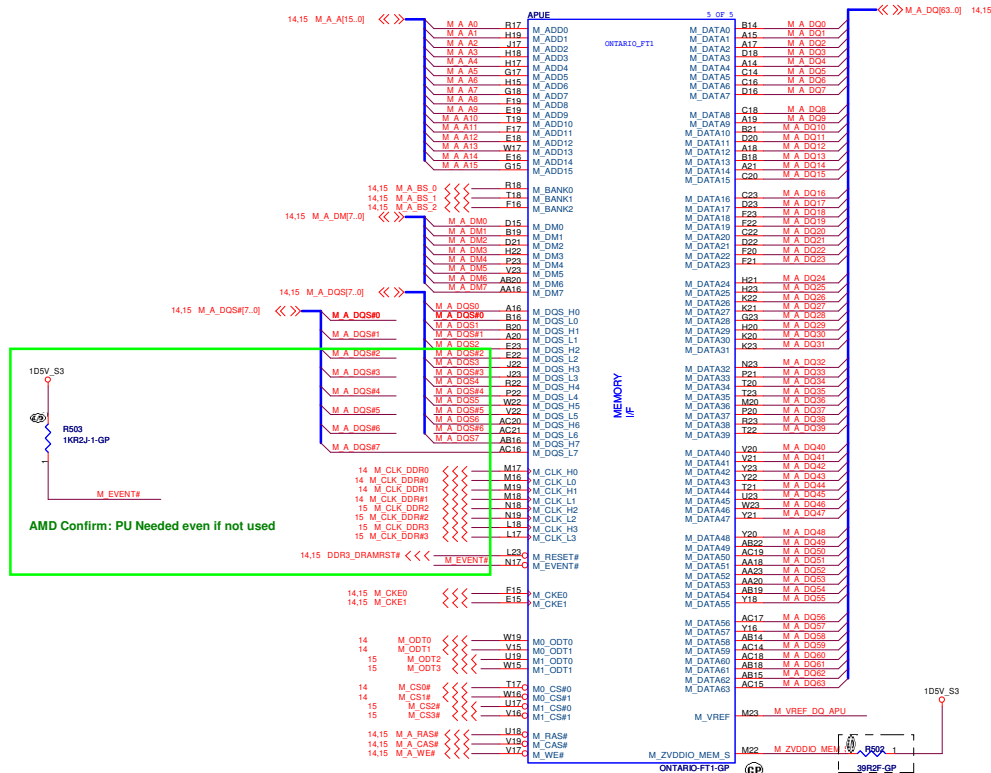
PCIe Routing

	APU
LANE0	PEG
LANE1	
LANE2	
LANE3	
	FCH
LANE0	LAN
LANE1	WWAN
LANE2	WLAN
LANE3	CardReader

TYPE ENABLED	EC_PWM2	EC_PWM3
Reserved	2.2-kohm 5% pull-down	2.2-kohm 5% pull-down
LPC ROM	Not connected.	2.2-kohm 5% pull-down
SPI ROM	2.2-kohm 5% pull-down	Not connected.
Reserved	Not connected.	Not connected.

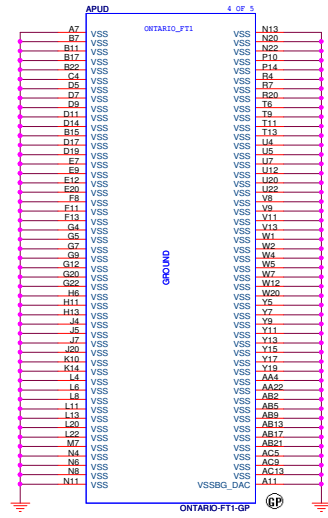
Note: EC\_PWM2, EC\_PWM3 default have internal 10kohm PU.





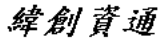




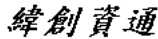




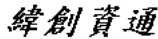
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Size	Document Number		Rev
	<b>B575</b>		<b>SA</b>
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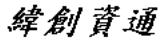
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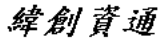
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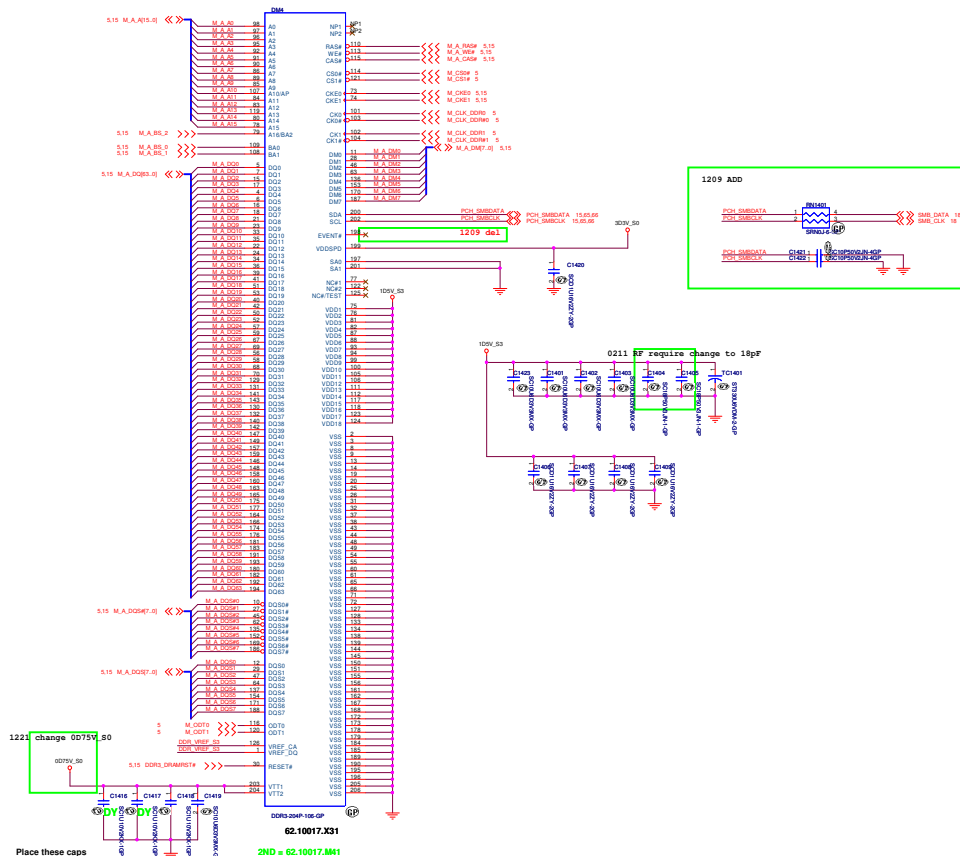
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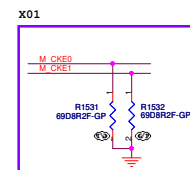
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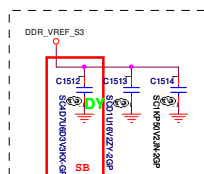
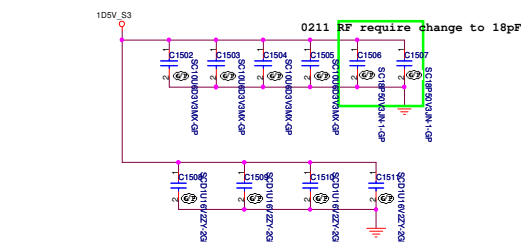
## DDR3 SOCKET\_1



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Intel HR DM tied to GND  
AMD still following previous design



1221 change 0D75V\_S0

0D75V\_S0

Place these caps close to VTT1 and VTT2

DY X-IGF DY X-IGF X-IGF 3MAX 2ND = 62.10017.P91

```
Intel HR B channel address is 01
AMD B channel address is 10
```

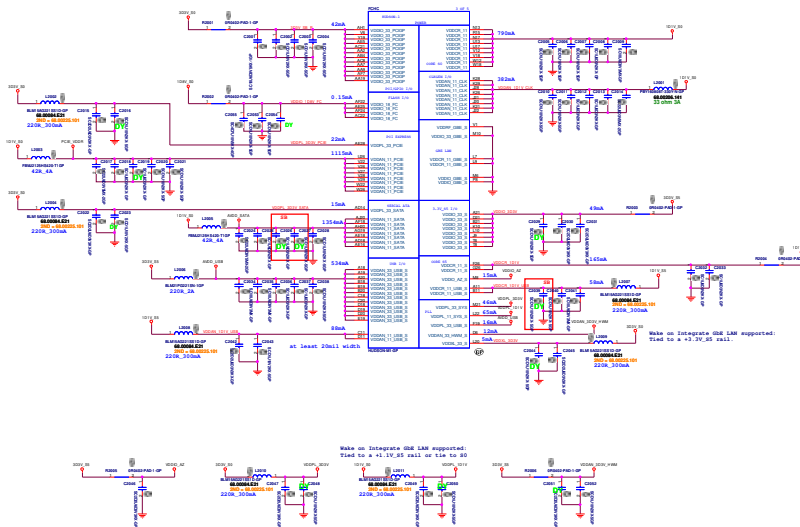








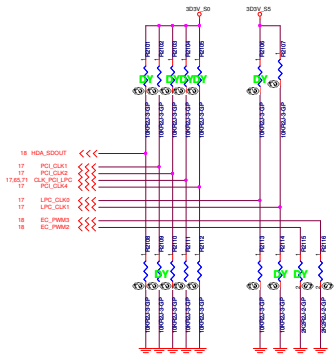




SSID = S.B

## REQUIRED STRAPS

CBP\_PU 3.3V\_AUX\_85  
checklist:PU 3.3V\_85  
confirm by AMD, following CBP suggestion



### REQUIRED SYSTEM STRAPS

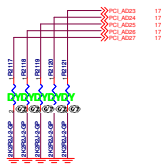
	AZ_S0OUT (AC2_S0DATAOUT_1)	PCI_CLK1	PCI_CLK2	PCI_CLK3 (CLK_PCI_LPC)	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	Low Power Mode	Allow PCE GEN2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC (Use Internal)	CLKGEN ENABLED (Use Internal)
PULL LOW	Performance Mode DEFAULT	Force PCE GEN1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

USE this pin to determine INT/EXT CLK

TYPE ENABLED	EC_PWM2	EC_PWM3
Reserved	2.2-kohm 5% pull-down	2.2-kohm 5% pull-down
LPC ROM	Not connected.	2.2-kohm 5% pull-down
SPIROM	2.2-kohm 5% pull-down	Not connected.
Reserved	Not connected.	Not connected.

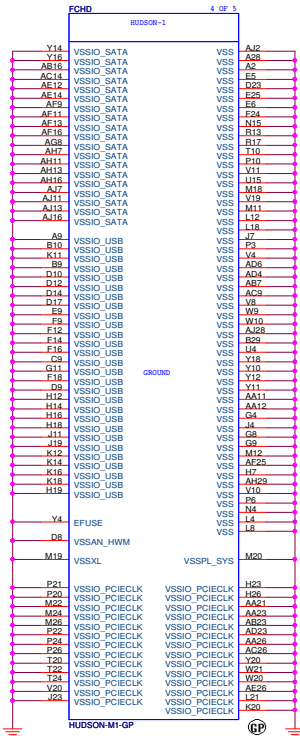
Note: EC\_PWM2, EC\_PWM3 default have internal 10kohm PU.

## DEBUG STRAPS



	PCI_AD27	PCI_AD28	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT POE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM POE STRAPS	Enable PCI MEM BOOT

Note: FCH has 15K internal PU FOR PCI\_AD[27:23]

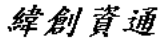


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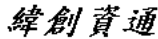
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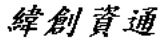
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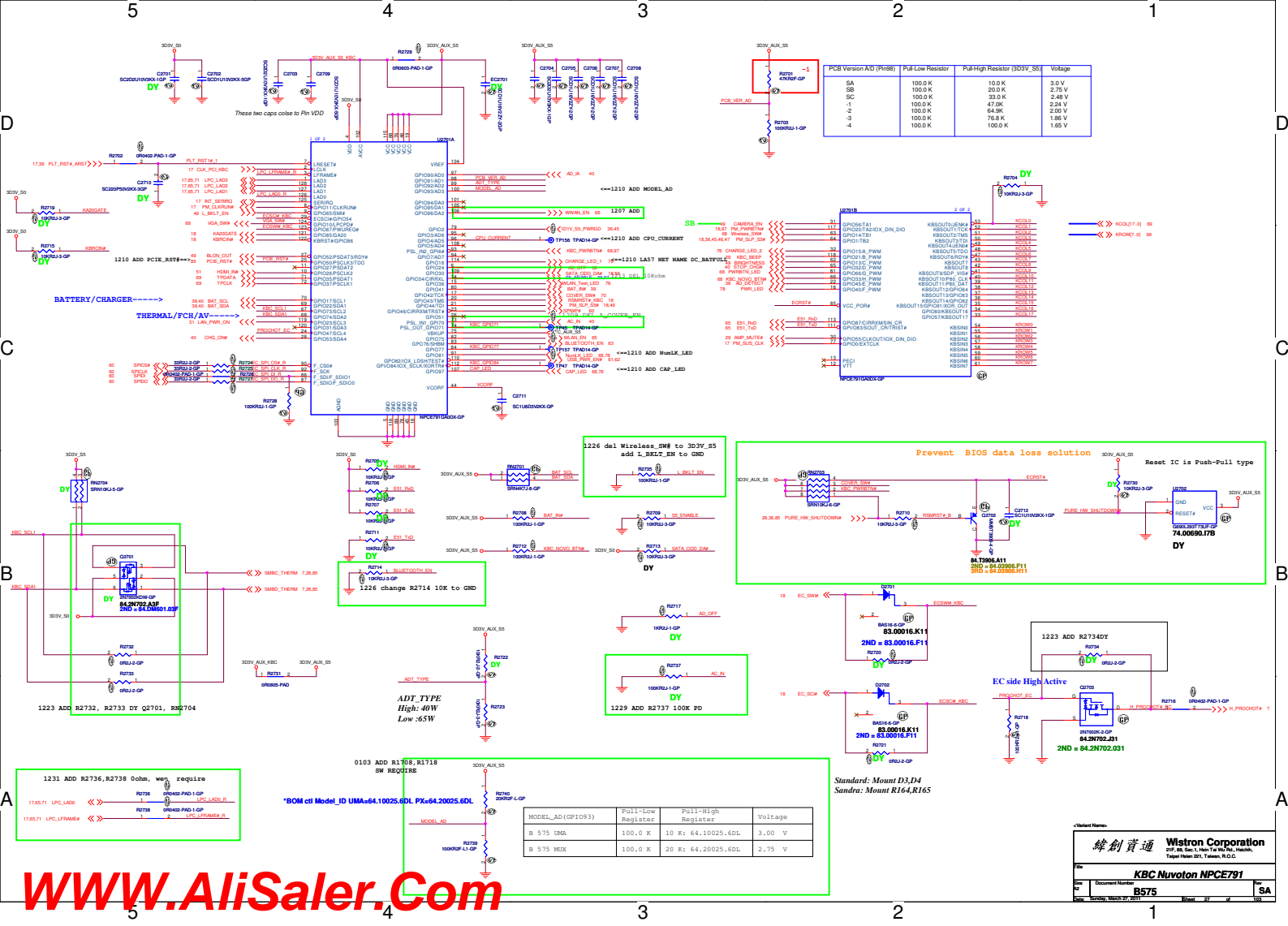
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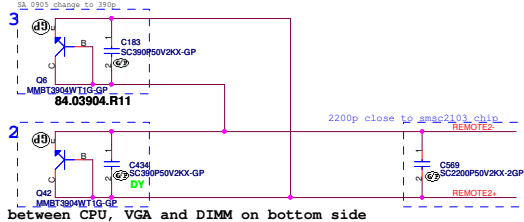
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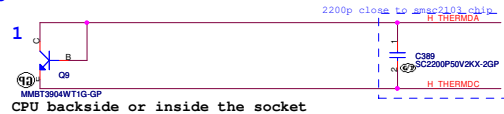
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Close to PCH on top side.



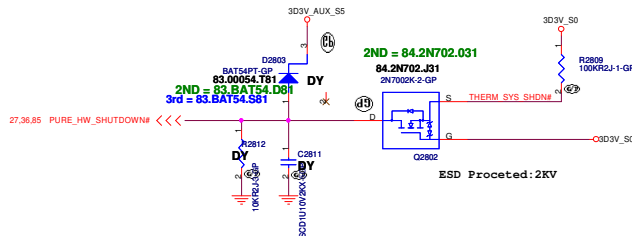
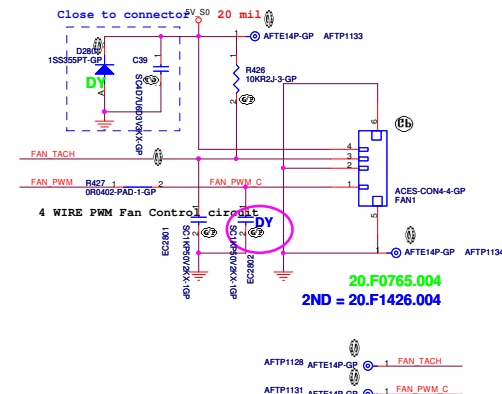
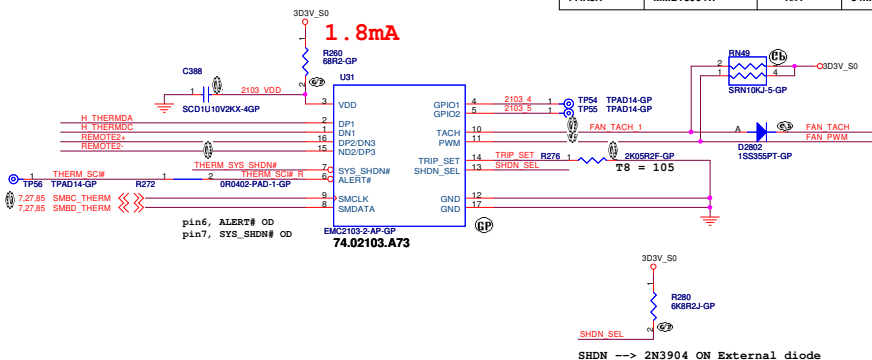
T8



CPU TEMP:  
H\_THERMDA and H\_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

Table 28.1- General Purpose Transistors multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ON	MMBT3904WT1G	N/A	84.03904.R11
PANJIT	MMBT3904W	N/A	84.M3904.A11



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<p>File Thermal/Fan Controller</p>	
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BOM Control



1209 ADD 2pcs 0805 short pad

place them under CODEC bottom

Port A: Headphone jack  
Port B:  
Port C: Microphone jack  
Port G: Internal stereo speakers  
Port J: Internal stereo digital mic

AUD\_PORTA\_R C R2930 1 5D1R2F-GP >> AUD\_PORTA\_R &

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**Codec**

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LA57 UMA

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**RTS5159 (CARD READER)**

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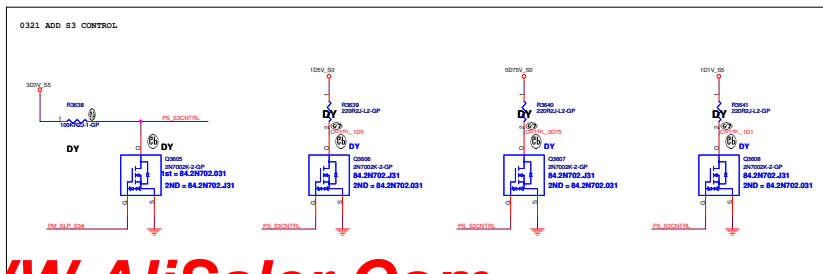
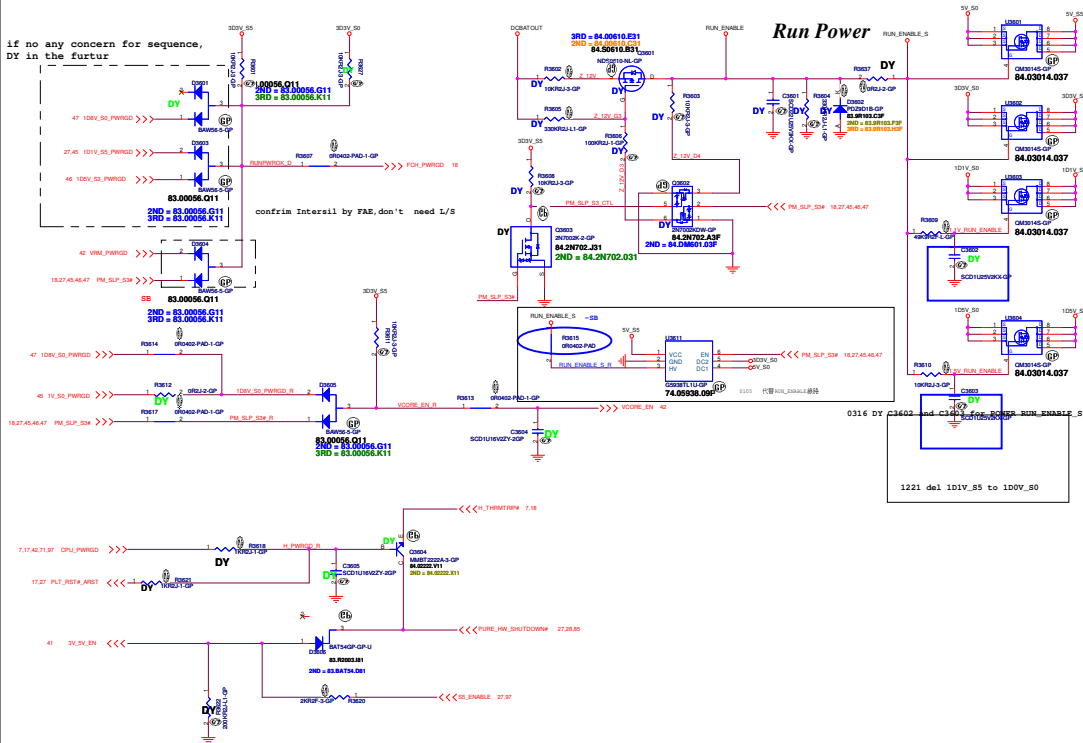
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USB3.0

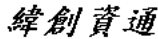
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if no any concern for sequence,  
DY in the furtur

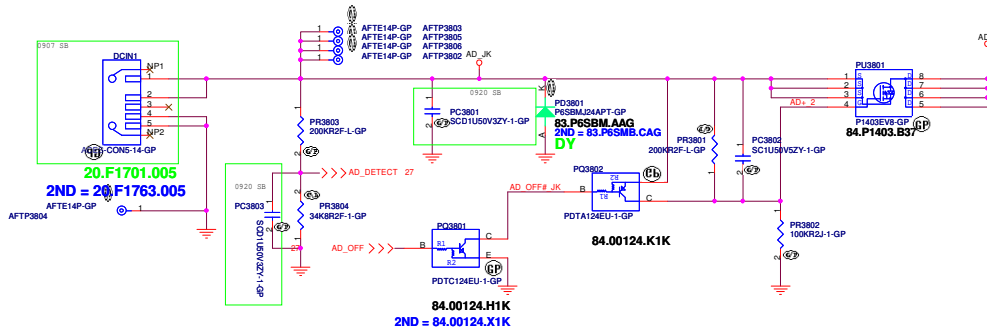


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## Adaptor in to generate DCBATOUT



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JV10-CS

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Title	<b>DCIN JACK</b>
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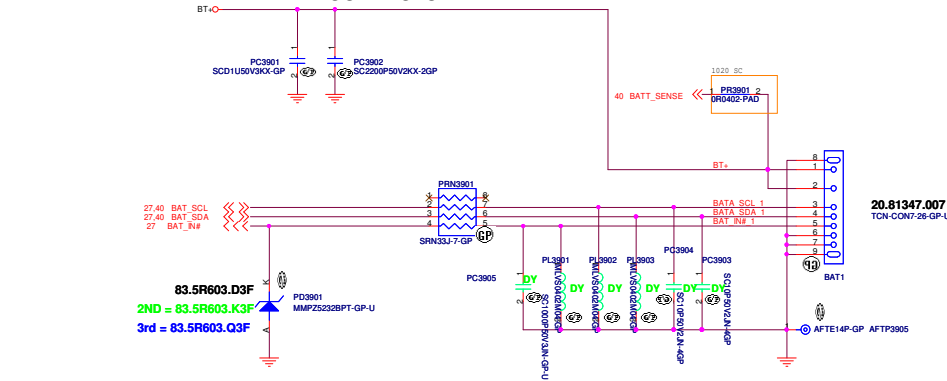
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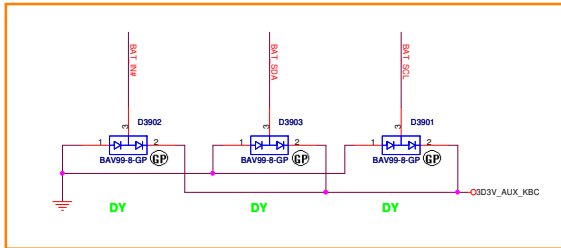
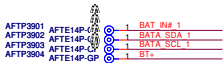
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Rev SA

# BATTERY CONNECTOR



20.81347.007  
TCN-C0N7-2S-GP-U



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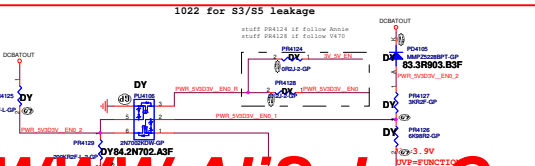
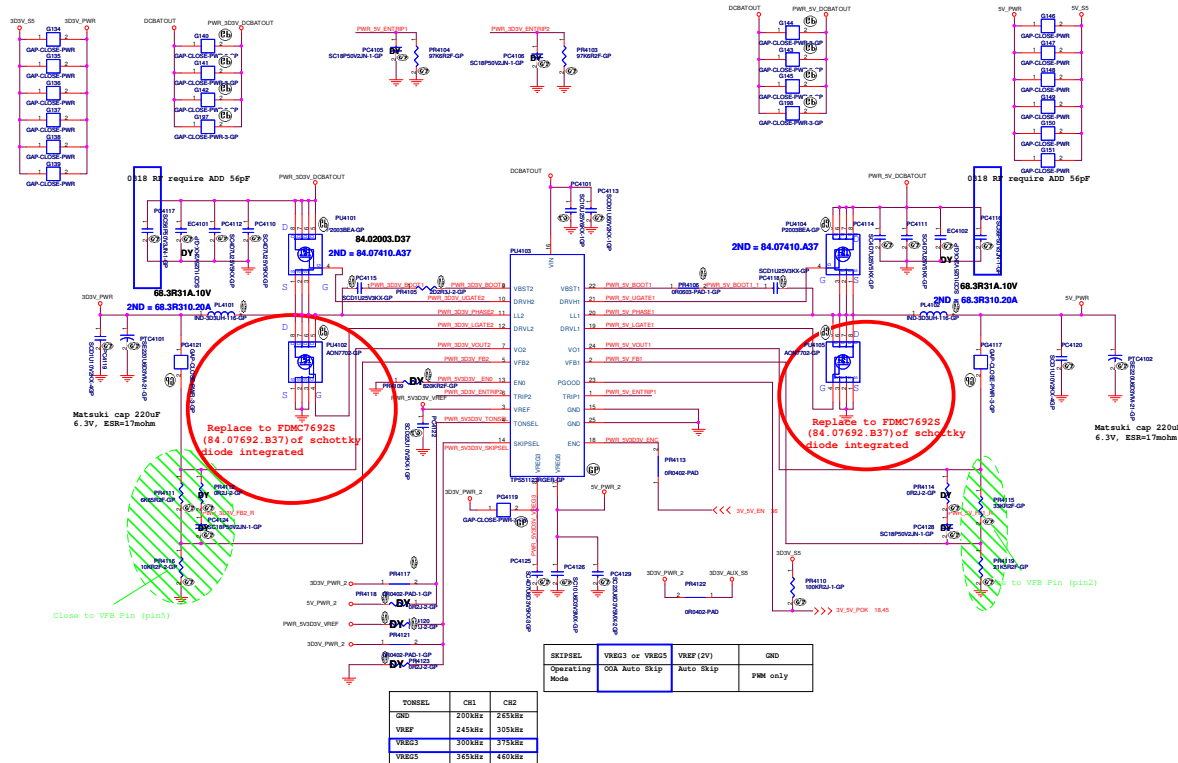
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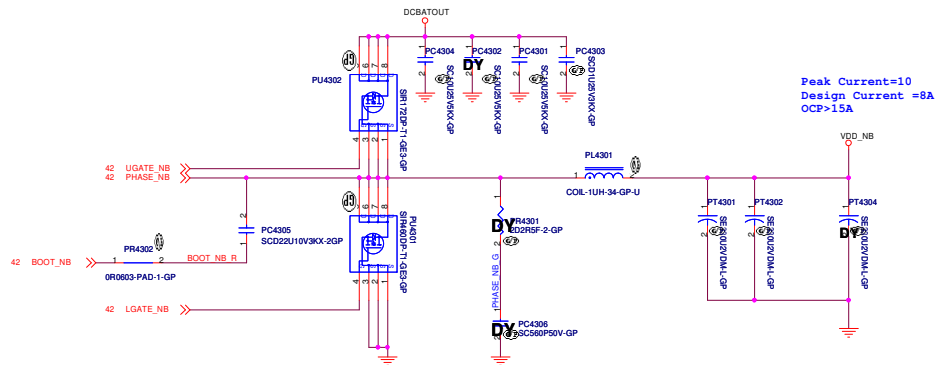


```
SSID = PWR.Plane.Regulator_5v3p3v
```



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I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: 1uH PCMC063T-1R0MN Cyntec 9mohm/10mohm Isat =22Arms 68.1R01A.20B  
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/79.33719.L01  
H/S: SIR712DF/ POWERPAK/ 10.3mOhm/12.4mOhm@4.5Vgs/ 84.00172.037  
L/S: SIR460DF/ POWERPAK/ 4.9mOhm/ 6.1mohm@4.5Vgs/ 84.00460.037

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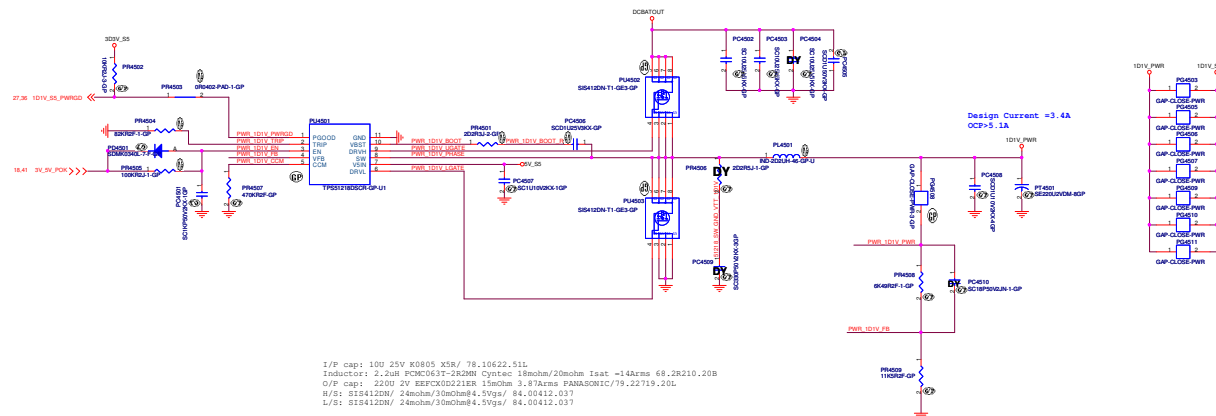
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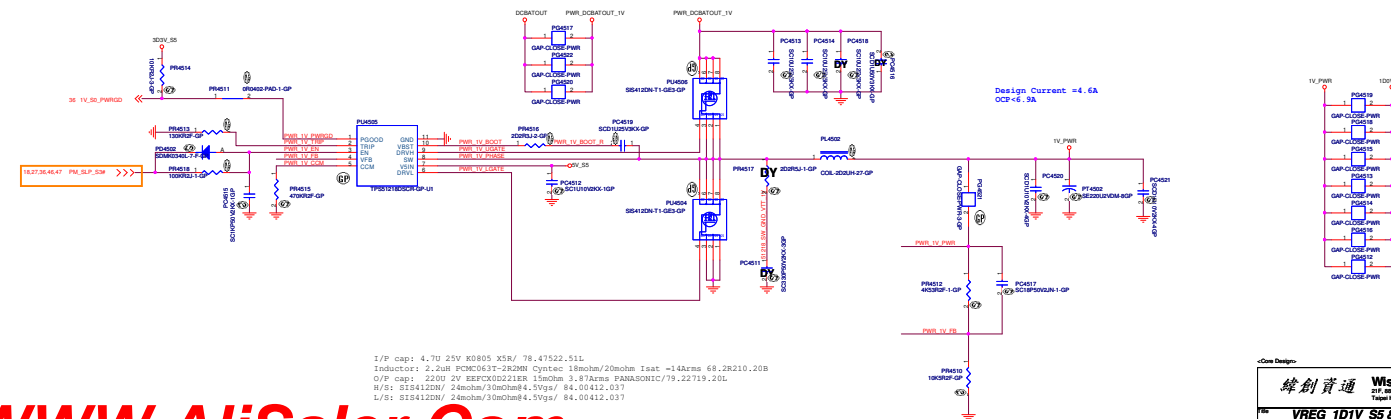
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SA	

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```
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```

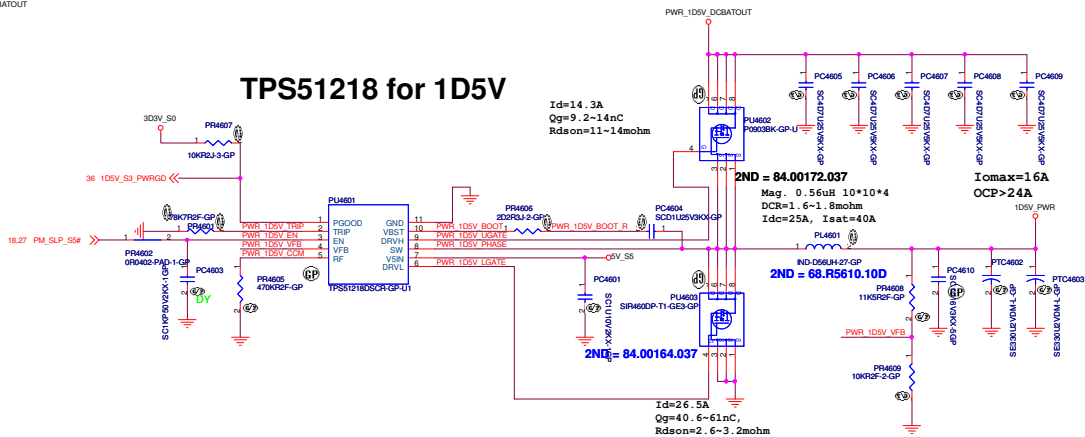


$$V_{out} = 0.704V * (R1 + R2) / R2$$

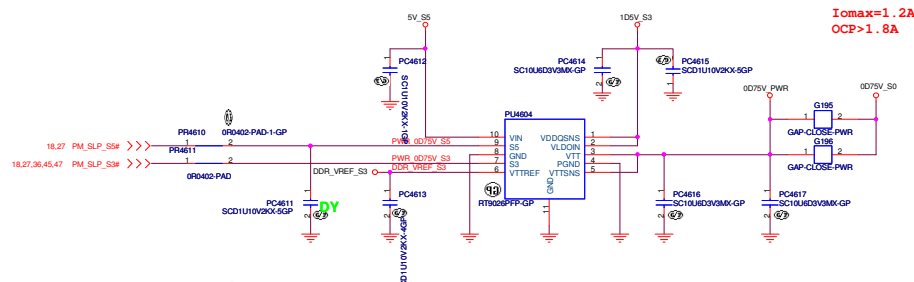


$$V_{out} = 0.704V * (R1 + R2) / R2$$

## TPS51218 for 1D5V



## RT9026 for 0D75V\_S3



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ITEM: **TPS51128 1D5V & RT9026PFP-GP 0D75V**

Doc: Document Number

Date: Monday, March 28, 2011


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Rev

SA



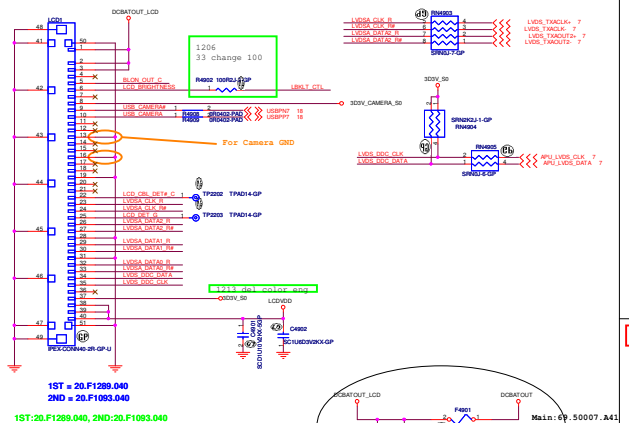
<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>G-Sensor</b>			
Size	Document Number		Rev
	<b>B575</b>		<b>SA</b>
Date: Friday, March 25, 2011		Sheet 48	of 103

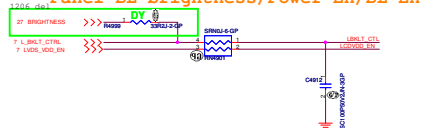


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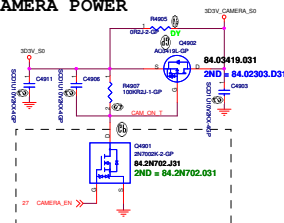
## LVDS CONNECTOR



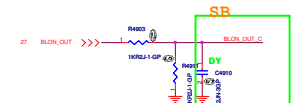
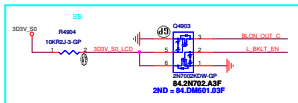
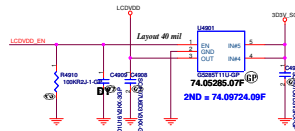
## Panel BL brightness/Power En/BL En



## CAMERA POWER



## SSID = VIDEO

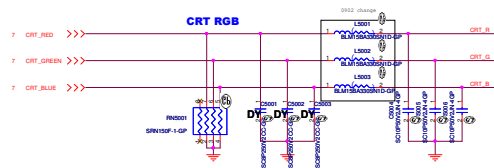


Core Design

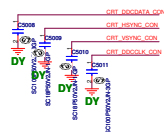
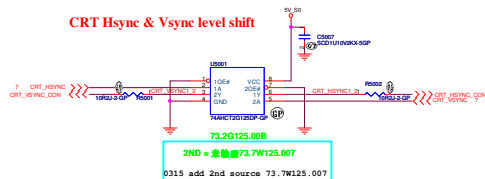
緯創資通 Wistron Corporation  
211, 8th, Sec.1, Hsin-Fu Rd, Taipei, R.O.C.

LCD Connector			Rev
Doc	Document Number		SA
Rev	B575		
Rev	Rev	Rev	Rev

WWW.AliSaler.Com



### CRT Hsync & Vsync level shift



**WWW.AliSaler.Com**

-SA 2nd = 22.10296.291



(Blanking)

(Blanking)

<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Tapei Hsien 221, Taiwan, R.O.C.	
Title			
<b>S-VIDEO</b>			
Size A4	Document Number <b>B575</b>		Rev <b>SA</b>
Date:	Friday, March 25, 2011		Sheet 53 of 103

(Blanking)

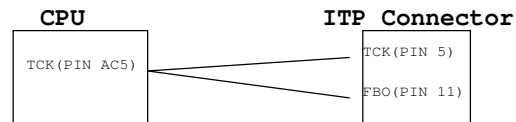
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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A4	B575		SA
Date:	Friday, March 25, 2011		Sheet 54 of 103

SSID = User.Interface

## ITP Connector

H\_CPURST# use pull-up Resistor close  
ITP connector 500 mil ( max ),  
others place near CPU side.



<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**ITP**

Size  
A4

Document Number

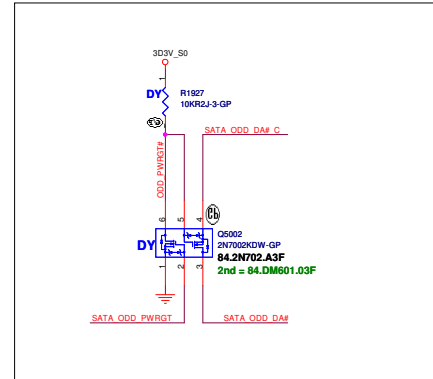
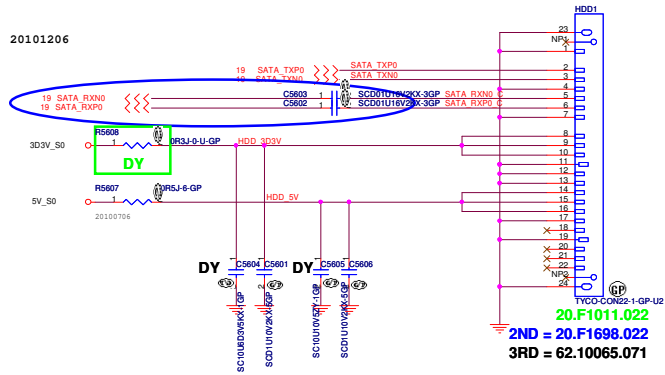
**B575**

Rev  
SA

Date: Friday, March 25, 2011

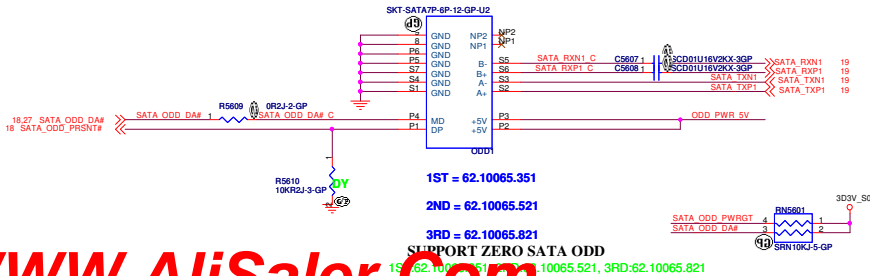
Sheet 55 of 103

## SATA HDD Connector

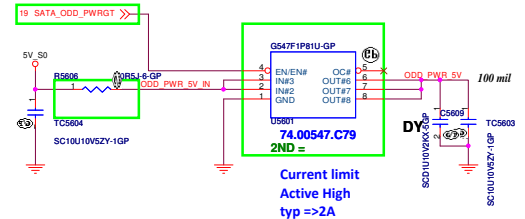


## ODD Connector

SATA\_RX- and SATA\_RX+ Trace  
Length match within 20 mil  
Mars:  
Exchange ODD and ESATA differential pair each other.



## SATA Zero Power ODD



&amp;ltCore Design&gt;

緯創資通

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**Title**

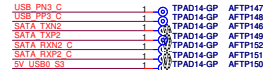
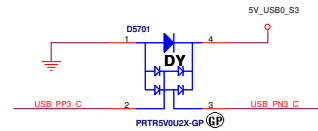
**HDD / ODD CONN**

**B575**

Rev

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29 AUD\_SPK\_L+L <<<  
29 AUD\_SPK\_L+L <<<

Place these EMI components  
close to speaker connector.

Only needed if speaker  
connector is physically far from  
audio codec. When in doubt, it's  
always a good idea to have  
population option.

EC5801  
SC100P50V2JN-3GP  
EC5802  
SC100P50V2JN-3GP

20100723 change



2ND = 20.F0693.002

1ST = 20.F1240.002

1ST:20.F1240.002, 2ND:20.F0693.002



2ND = 20.F0693.002

1ST = 20.F1240.002

1ST:20.F1240.002, 2ND:20.F0693.002

AFTP138 AFTE14P-GP 1 AUD\_SPK\_L+L  
AFTP137 AFTE14P-GP 1 AUD\_SPK\_L+L  
AFTP129 AFTE14P-GP 1 AUD\_SPK\_R+L  
AFTP140 AFTE14P-GP 1 AUD\_SPK\_R+L

29 AUD\_SPK\_R+L <<<  
29 AUD\_SPK\_R+L <<<

EC5803  
SC100P50V2JN-3GP  
EC5804  
SC100P50V2JN-3GP

<Core Design>

緯創資通

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

File		<b>SPEAKER</b>	
Size	Document Number	B575	
A3		SA	
Date:	Modified: March 28, 2011	Sheet	58 of 100

Reserved

<Core Design>

緯創資通

Wistron Corporation

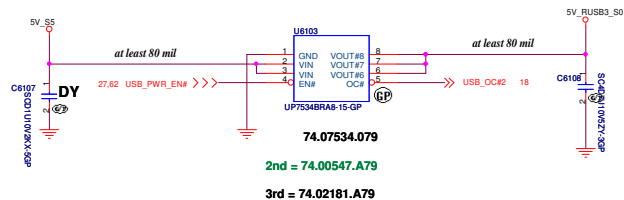
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

File		
Reserved		
Size	Document Number	Rev
43	B575	SA
Date: Friday, March 25, 2011		
Sheet 59 of 103		

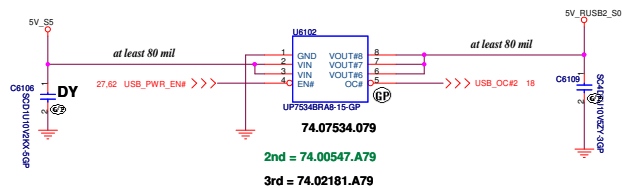


SSID = USB

## RJ45\_USB Board USB Power



## I/O Board USB Power



<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

File

**USB Power SW**

Size

Document Number

**B575**

Rev

**SA**

Date: Monday, March 28, 2011

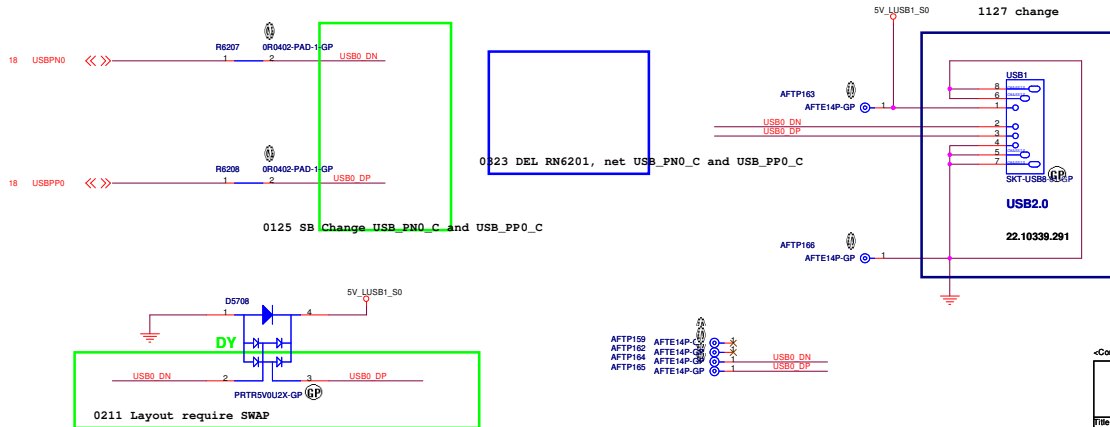
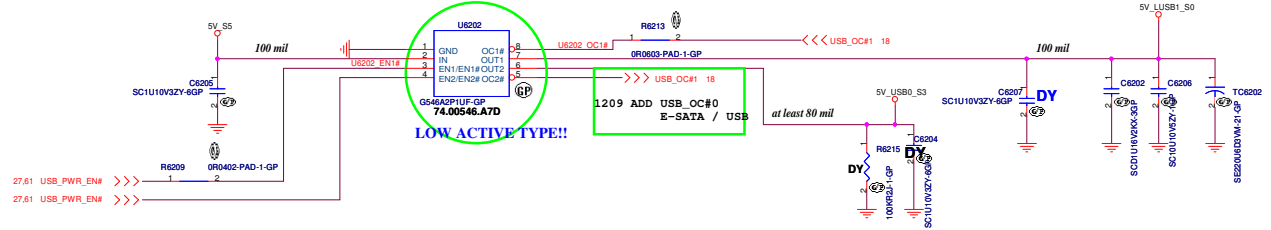
Sheet

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of

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## Left Side USB Power Switch

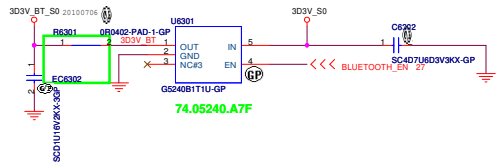


**<Core Design>**

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

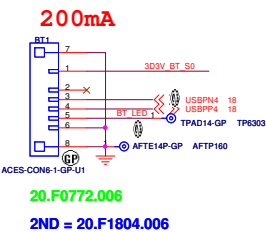
Title			
<b>USB CONN</b>			
Size	Document Number		Rev
	<b>B575</b>		<b>S</b>
Date: Monday, March 28, 2011		Sheet 62 of	103

Bluetooth Power



BT CONN.

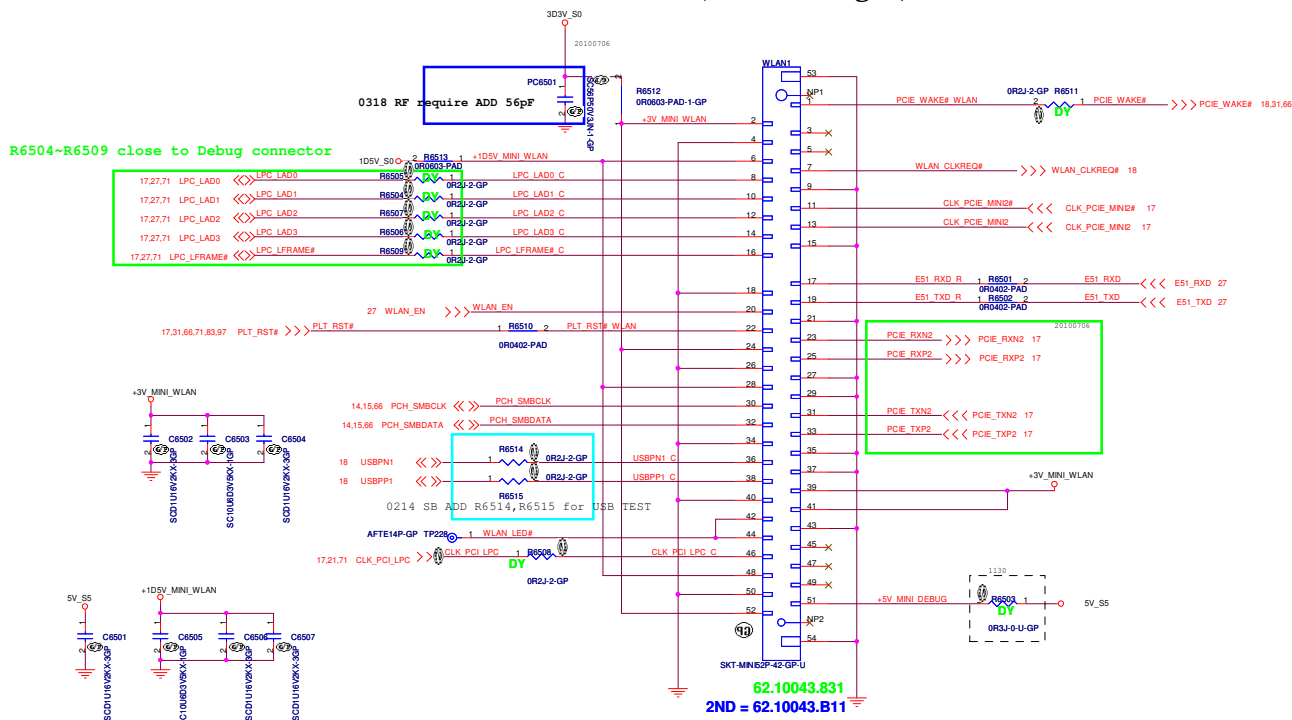
EC6302 put near  
BLUE1 / all USB  
put one choke  
near connector  
by EMI request







### **Mini Card Connector(802.11a/b/g/n)**



◀Core Design:

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466
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## MINICARD WLAN

Size

Document Number
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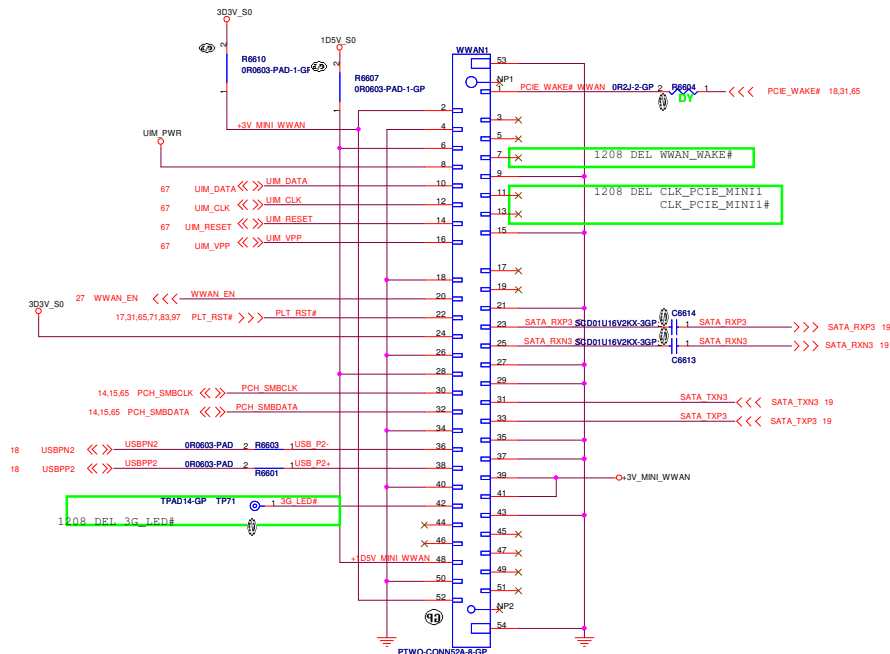
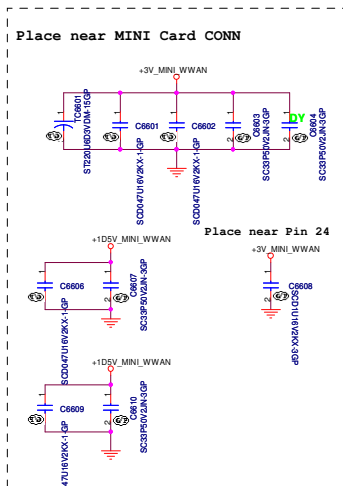
Rev

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**WWW.AliSaler.Com**

### **Mini Card Connector(WWAN)**



&lt;Core Design&gt;

緯創資通

**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Item	Value
1. Title	

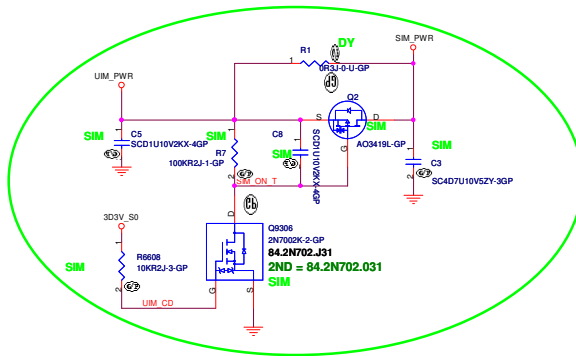
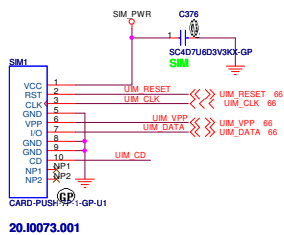
**MINICARD WWAN**

Rev

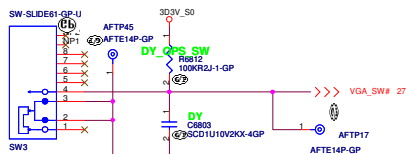
Size	Document Number
	<b>B575</b>

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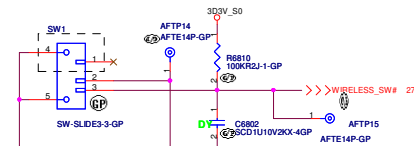
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DY\_OPS\_SW  
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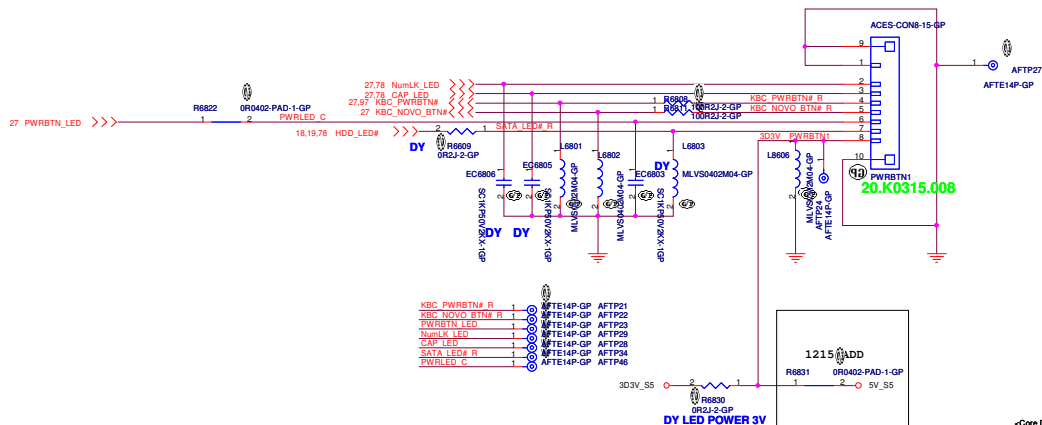


```
1208 ADD VGA SW
```



62.40018.491

1208 ADD BT SW



### ◀Core Design▶

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

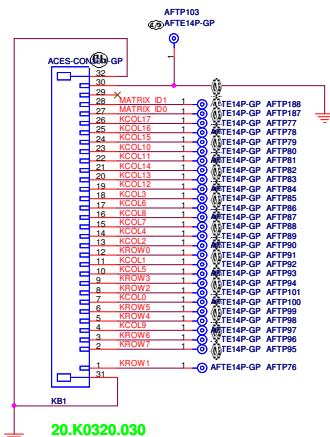
Rev

### POWER BUTTON

B575

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## Internal KeyBoard Connector



S205少雨PIN,  
原為測點已補上

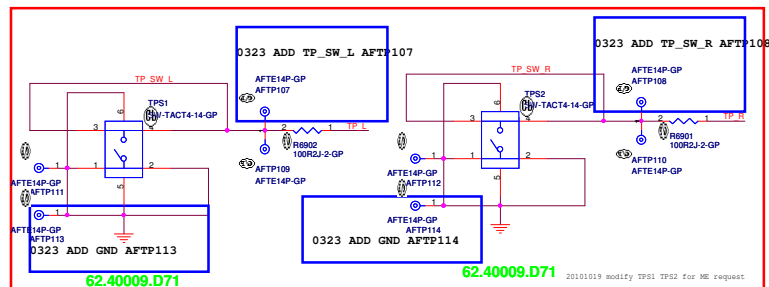
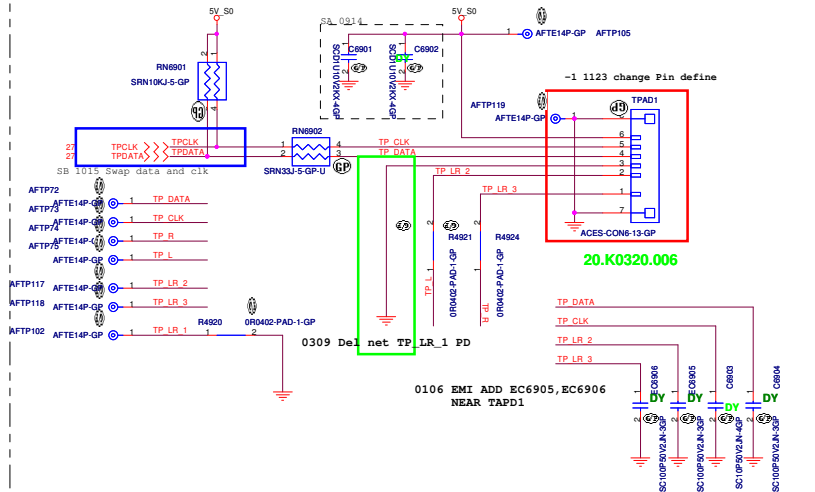
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	27	28	29	30
	ID0	ID1	ID2	GND
<b>US</b>	GND	GND	X	GND
<b>GB</b>	GND	X	X	GND
<b>JP</b>	X	GND	X	GND

— <> KROW[7..0] 27

— <> KCO417..0] 27

20.K0320.030

```
SSID = Touch.Pad
```



20101019 modify TPS1 TPS2 for ME request

•Core Design:

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

IT 100

**KB/TP CONN**

Size

Document Number

Rev

A3

B575

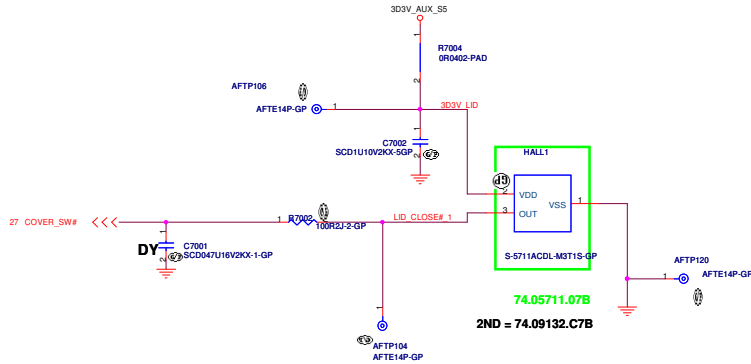
2

Date: Monday

Sheet

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# Hall Sensor

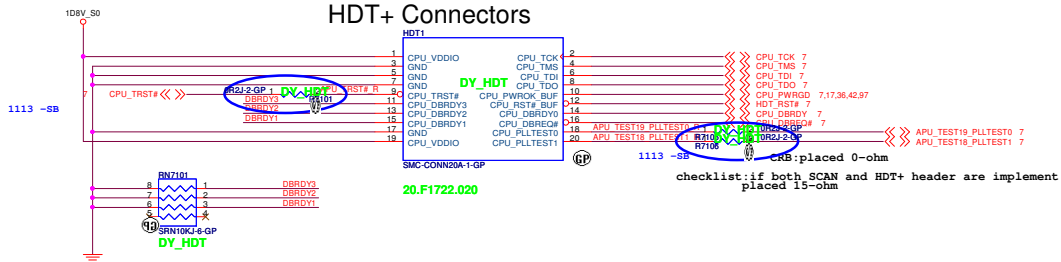


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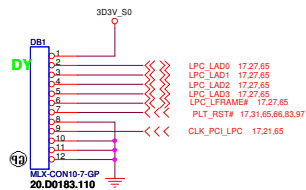
緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,  
Taipai Hsien 321, Taiwan, R.O.C.

File		Rev
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<b>HALL Sensor</b>		
<b>B575</b>		
Date: Monday, March 28, 2011	Sheet 70 of 103	



## GOLDEN FINGER FOR DEBUG BOARD



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LA57 UMA

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Tapei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size A4	Document Number <b>B575</b>		Rev <b>SA</b>
Date: Friday, March 25, 2011		Sheet 72	of 103



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LA57 UMA

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size A4	Document Number <b>B575</b>		Rev <b>SA</b>
Date: Friday, March 25, 2011	2	Sheet 73 of 103	1

LA57 UMA

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Tapei Hsien 221, Taiwan, R.O.C.	
Title			
<b>CARD Reader CONN</b>			
Size A4	Document Number <b>B575</b>		Rev <b>SA</b>
Date: Friday, March 25, 2011		Sheet 74	of 103

LA57 UMA

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Tapei Hsien 221, Taiwan, R.O.C.	
Title			
<b>New Card</b>			
Size A4	Document Number <b>B575</b>		Rev <b>SA</b>
Date: Friday, March 25, 2011		Sheet 75	of 103

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LA57 UMA

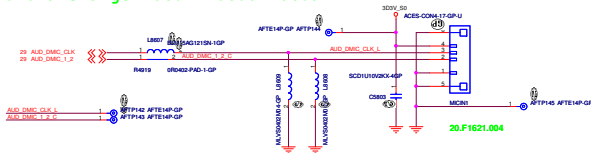
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,		Tapei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size	Document Number		Rev
A4	<b>B575</b>		<b>SA</b>
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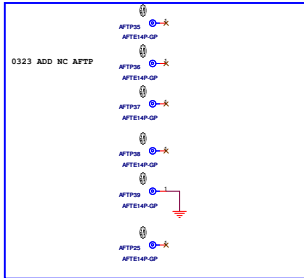
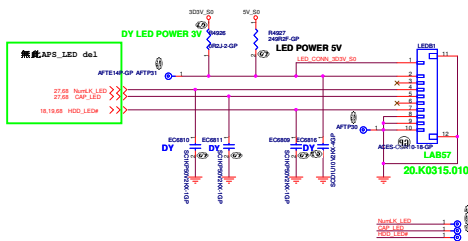
LA57 UMA

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Title			
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Size A4	Document Number <b>B575</b>		Rev <b>SA</b>
Date: Friday, March 25, 2011		Sheet 77	of 103

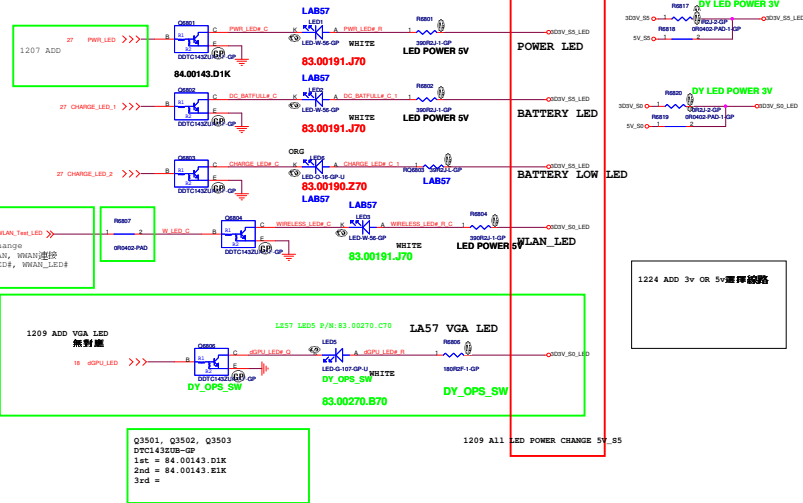
20101019 change L8607 L8608 L8609



### LED BORD CONN.



LED



Core Design

緯創資通

Wistron Corporation

21F, 8F, 5th, 1, 10th, 11th, 12th, 13th, 14th, 15th, 16th, 17th, 18th, 19th, 20th, 21st, Taiwan, R.O.C.

REFERENCE

Document Number

B575

Date: Monday, March 24, 2011

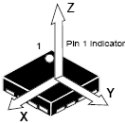
SA

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	ADXL322	
	LIS244AL	No Accel
	LIS34AL	
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

STMicro LIS34AL: 74.00034.0BZ  
ADXL335 : 74.00335.0BZ

Layout Comment :  
(1) Place C483, C484, Q46, R528, R530,  
C479, C476, R509, R508 close to U55.  
(2) Avoid routing under DCDC switching area.



(Blanking)

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Title			
<b>Reserved</b>			
Size A4	Document Number <b>B575</b>		Rev <b>SA</b>
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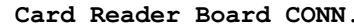


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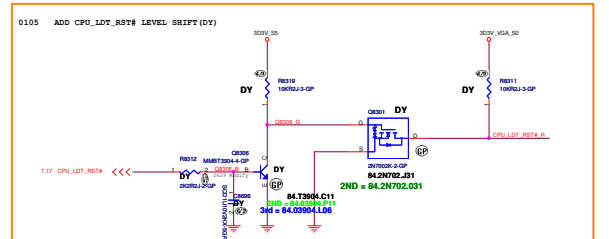
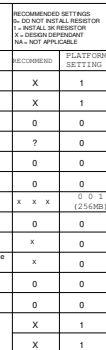
LA57 UMA

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Tapei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size	Document Number		Rev
A4	<b>B575</b>		<b>SA</b>
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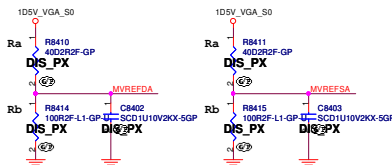
RJ45\_USB\_CONN.



Title			
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Size	Document Number		Rev
	<b>B575</b>		<b>SA</b>
Date:	Monday, March 28, 2011	Sheet 82 of	103



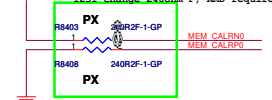
# PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



## DDR3/GDDR3 Memory Stuff Option (ROBSON-S3/SEYMOUR-XT-S3)

	DDR5	DDR3
MVDDQ	1.5V	1.5V/1.8V
Ra	40.2R	40.2R
Rb	100R	100R

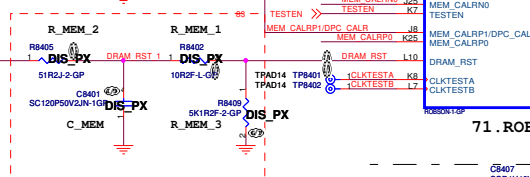
1231 change 240ohm F, AMD require  
DPC\_CALR (Park/Robson-S3):  
Analog calibration.  
Connect DPx\_CALR to GND through a 150-Q (1%) resistor.



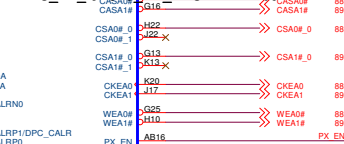
★ This basic topology should be used for DRAM\_RST for GDDR3/GDDR5/DDR5. These Capacitors and Resistor values are an example only. The Series R and I Cap values will depend on the DRAM Load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec.

Designator	For SEYMOUR	For Robson
R_MEM_1	10R	10R
R_MEM_2	50R	50R
R_MEM_3	5K	5K
C_MEM_1	120p	120p

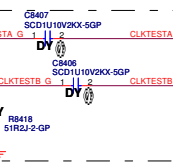
Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except R\_MEM\_2



## DIS\_PX lenovo PN 71.SEYMR.M09



## 71.ROBSON.M12 Colay with Seymour-XT-S3 (71.SEYMR.M01)



2010/07/06  
Schematics check list:  
A pull-down resistor is required.

~Variant Name~

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File: GPU Memory(2/5)  
Doc Number: B575  
Date: Monday, March 28, 2011 Sheet 84 of 103

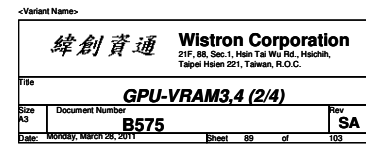




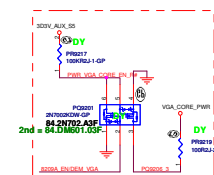
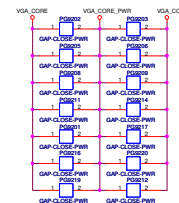
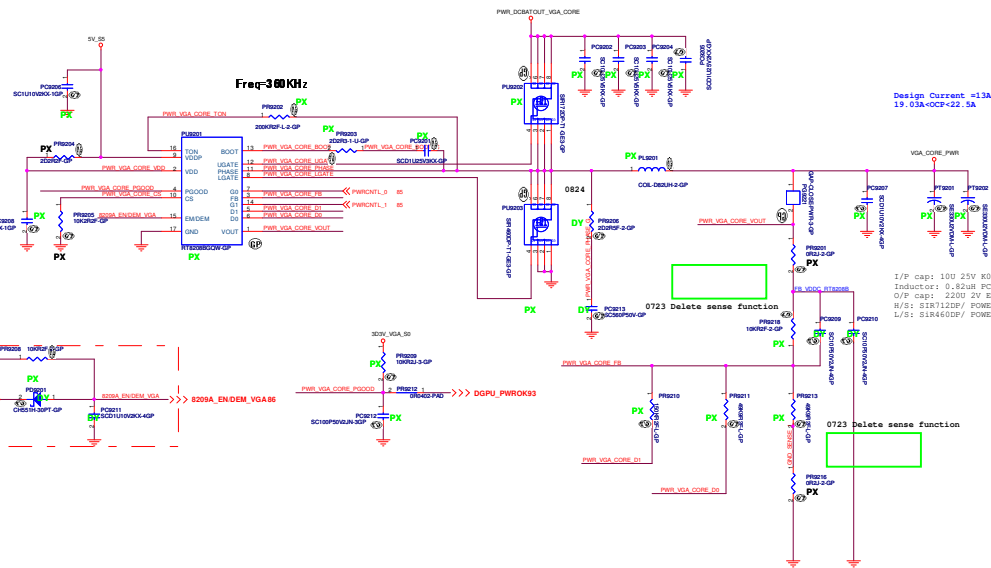
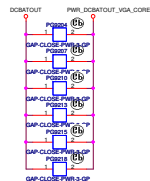








```
SSID = PWR.Plane.Regulator_VGACORE
```



RMS MDI CORE D1	RMS MDI CORE D0	MDI CORE RMS
5	5	1.9501
5	11	0.000
11	7	0.0001
11	11	0.0001

Seymour-XT		
FWR_VGA_CORE_D1	FWR_VGA_CORE_D0	VGA_CORE_FWR
L	L	1.1V
H	H	0.85V
H	L	1.05V
H	H	0.9V

$$V_{out} = 0.75V * (R1 + R2) / R2$$

For ROBSON

PR9210=44K.2K(64.44225.6DL)

PR0211=150K (64.15035.6DL)

cCore Design

緯創資通 Wistron Corporation

File **RT8208B +VCC GFXCORE**

B579

Page
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PR0211-150K (64.15035.6DL)

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[illegible]

	PE_GPIO0	PE_GPIO1
dGPU mode	H	H
IGPU	L	L
IGPU with BACO	H	H

[illegible]

10DV\_S0 should ramp-up before 1V\_VGA\_S0  
 1V\_VGA\_S0 should ramp-up before 10DV\_S0 falls  
 so 1V\_VGA\_S0 EN have to fine tune RC delay after VGA Core

0629 Modify:  
Reserved PD9202 connect DGPU\_PWR\_EN to  
PWR\_TV\_EN for power down sequence.

17.32 PE\_GPI01

DY PD9202

CH651H-30PT-GA

Vo(cal.)=1.0036V

TV\_VGA\_PWR

TV\_VGA\_S0

PC0102

PC0317

PC0316

PC0201

PC0202

PC0203

PC0204

PC0205

PC0206

PC0207

PC0208

PC0209

PC0210

PC0211

PC0212

PC0213

PC0214

PC0215

PC0216

PC0217

PC0218

PC0219

PC0220

PC0221

PC0222

PC0223

PC0224

PC0225

PC0226

PC0227

PC0228

PC0229

PC0230

PC0231

PC0232

PC0233

PC0234

PC0235

PC0236

PC0237

PC0238

PC0239

PC0240

PC0241

PC0242

PC0243

PC0244

PC0245

PC0246

PC0247

PC0248

PC0249

PC0250

PC0251

PC0252

PC0253

PC0254

PC0255

PC0256

PC0257

PC0258

PC0259

PC0260

PC0261

PC0262

PC0263

PC0264

PC0265

PC0266

PC0267

PC0268

PC0269

PC0270

PC0271

PC0272

PC0273

PC0274

PC0275

PC0276

PC0277

PC0278

PC0279

PC0280

PC0281

PC0282

PC0283

PC0284

PC0285

PC0286

PC0287

PC0288

PC0289

PC0290

PC0291

PC0292

PC0293

PC0294

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PC0296

PC0297

PC0298

PC0299

PC0300

PC0301

PC0302

PC0303

PC0304

PC0305

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PC0307

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PC0372

PC0373

PC0374

PC0375

PC0376

PC0377

PC0378

PC0379

PC0380

PC0381

PC0382

PC0383

PC0384

PC0385

PC0386

PC0387

PC0388

PC0389

PC0390

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PC0399

PC0400

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PC0445

PC0446

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PC0450

PC0451

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PC0459

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PC0500

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PC0504

PC0505

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PC0509

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PC0521

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PC0530

PC0531

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PC0534

PC0535

PC0536

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PC0539

PC0540

PC0541

PC0542

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PC0546

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PC0548

PC0549

PC0550

PC0551

PC

$$V_{out} = 0.8V * (R1 + R2) / R2$$

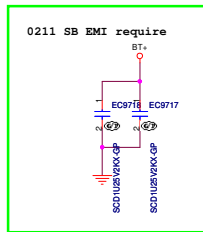
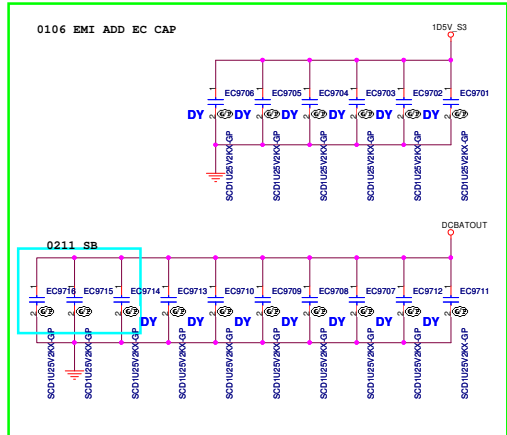
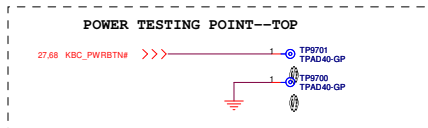
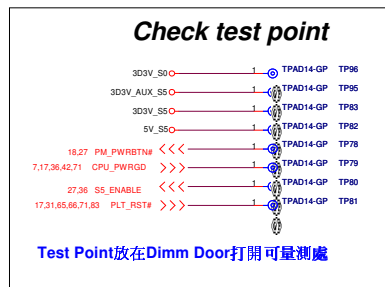
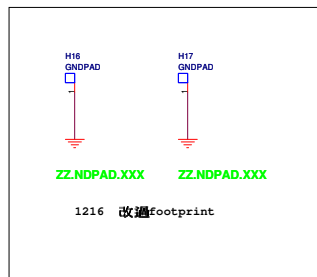
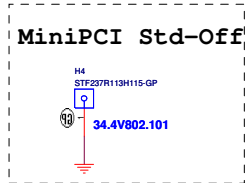
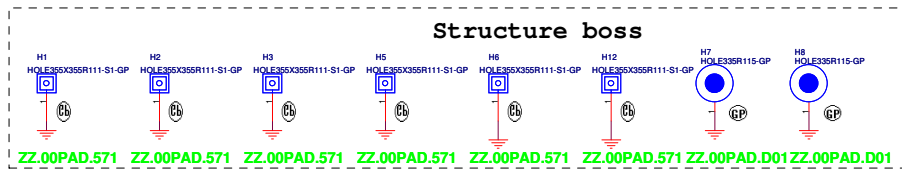
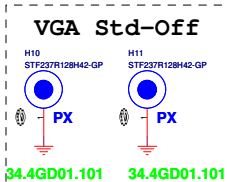
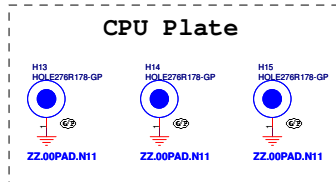
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichia,		Taipei Hsien 221, Taiwan, R.O.C.	
File			
HDD / ODD CONN			
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<Variant Name>		
<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
CRT Switch		
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LA57 UMA

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Title			
<b>TOUCH PANEL</b>			
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待確認

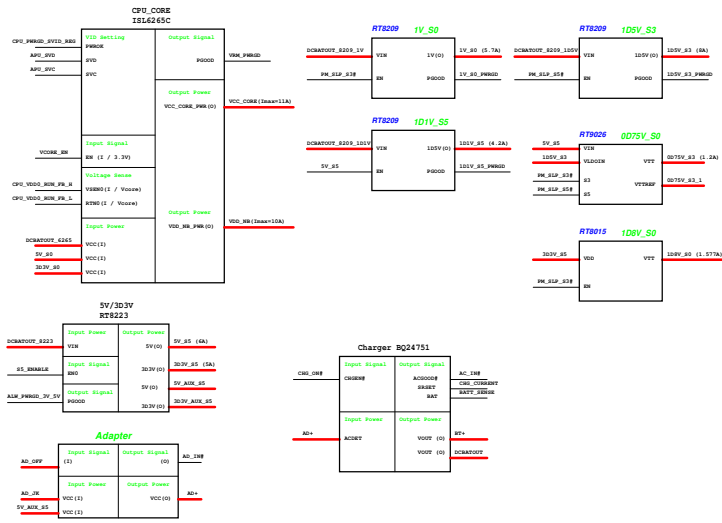
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Title			
Change History			
Size	Document Number		Rev
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待確認



# Power Delivery Block Diagram

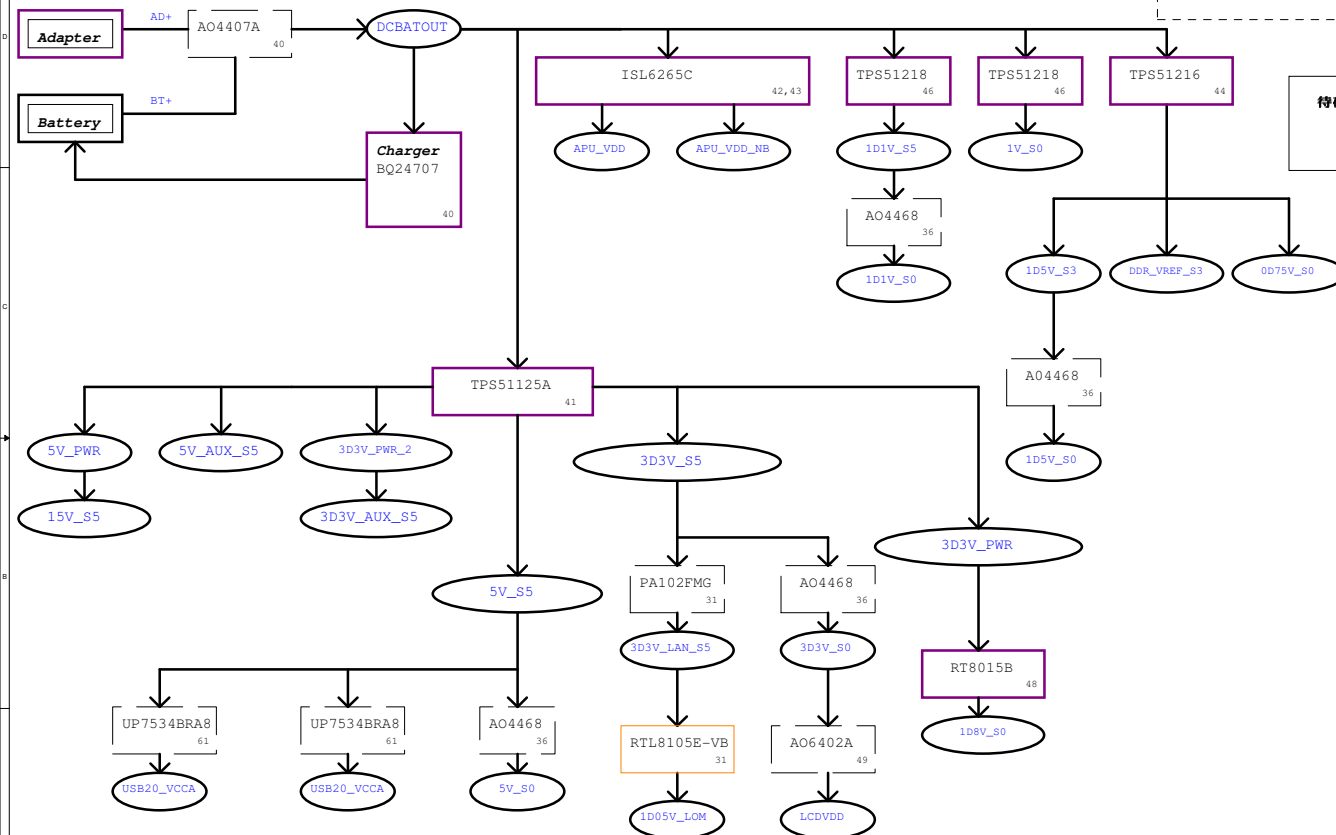
Power Shape

Regulator

LDO

Switch

待確認

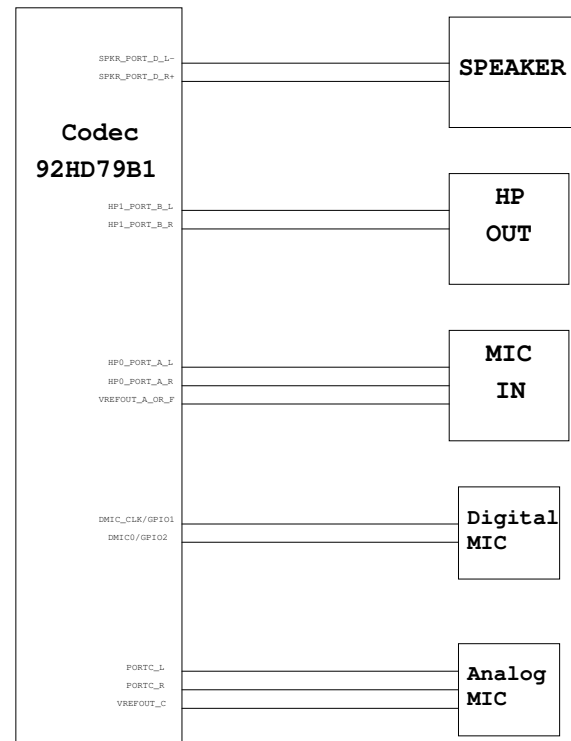
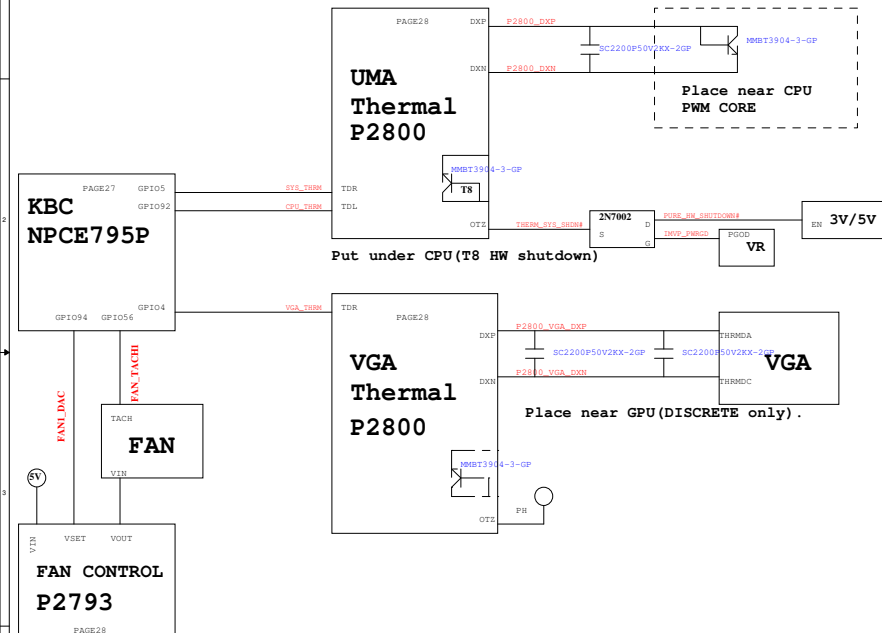


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File	Power Block Diagram		
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## Audio Block Diagram



&amp;ltCore Design&gt;

緯創資通

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Title

### Thermal/Audio Block Diagram

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Custom	

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<Variant Name>

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Document Number

Rev

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